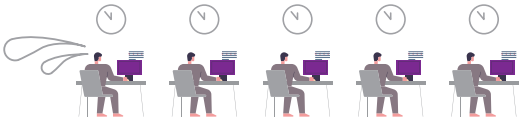
INDUSTRY'S FASTEST CHIP-LEVEL POWER ANALYZER



PowerBaum is a state-of-the-art, highly accurate power analysis solution that enables designers to optimize the power consumption of their semiconductor designs. It employs the design's source description files (RTL and netlist) to generate a high-performance power model.

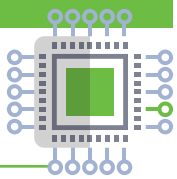
PowerBaum relies on sample gate-level power simulations to build and train the model with gate-level power analysis accuracy. PowerWurzel is Baum's gate-level simulation engine used to train Baum power models. Combining PowerWurzel with PowerBaum creates a powerful and efficient flow to generate extremely fast and accurate power models. PowerWurzel can also accept RTL FSDB/VCD and internally generate gate-level signal vectors. This is a convenient option when gate-level vectors are not ready in the early stage of the design.

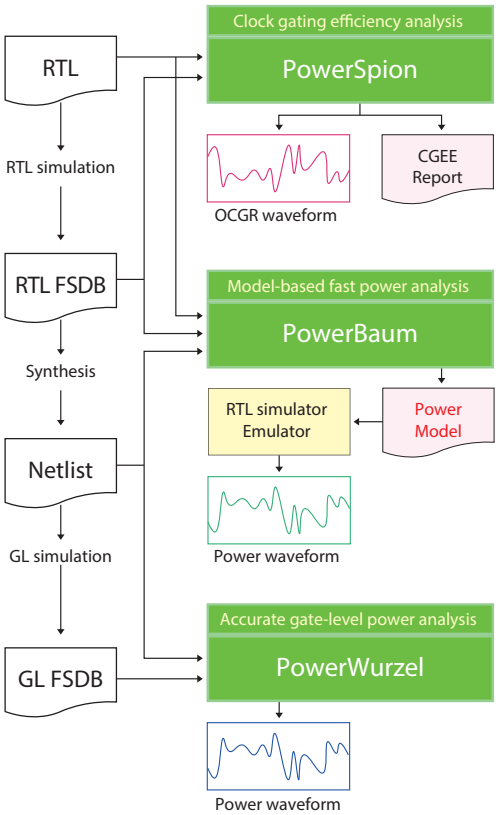
Once the power model is trained, it can be used in many simulation environments executing large workloads with a high level of accuracy. Baum power models integrate into RTL simulations, ESL/virtual platforms, or emulation to achieve orders of magnitude performance improvement compared to competing solutions in the market. This creates the best of both worlds achieving the highest speeds in the industry while maintaining very high accuracy.

PowerBaum enables designers to perform power analysis with multiple different realistic scenarios or even under real software loads. With Baum power models, designers can analyze both transient and average power to identify and isolate power issues in the design and fix them.

SOFTWARE POWER ANALYSIS SUITE

- Best-in-class technology
- 100x faster than competing solutions
- Gate-level accuracy
- RTL/ESL simulations & hardware emulation integration
- Power analysis at earlier design stage
- Completely automated





PowerSpion

- Clock gating efficiency analysis of RTL source
  - Fast clock gating inference
  - Offer clock gating report CGE, CGR, CGEE, OCGR
- Offer power optimization guidelines
  - Suggest minimum_bitwidth for optimum clock gating
  - Redundancy detection and removal from RTL source

PowerBaum

- Extremely fast power analysis using power model
  - Fast power waveform extraction
- Automatic power modeling
- Support emulator power analysis
- Automatic extraction of power equation

PowerWurzel

- Accurate gate-level power analysis
- Automatic conversion from RTL FSDB to GL FSDB
- Clock mesh analysis
- Multiple VT corner analysis

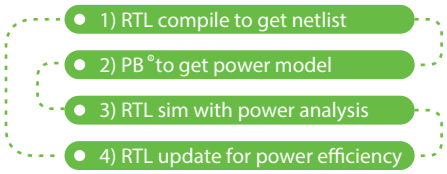
BAUM

POWERBAUM FEATURES

- Design hierarchy support (power models at any level of the hierarchy)
- Parallel power modelling
- Power analysis with multiple power models
- Baum Emulator PM: power model in a form of hardware
- Power optimization guidelines
- Support for multi-clock, multi-VDD and dynamic frequency scaling
- Power analysis of multiple instances with one power model
- Power analysis across VDD/temperature variations

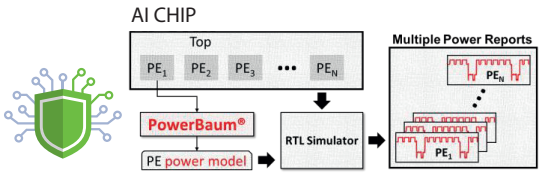
RTL OPTIMIZATION

Early power-related design decisions have the most potential to minimize power consumption in a semiconductor design. Integration of PowerBaum into RTL simulation is very easily making it very feasible for RTL optimization. Therefore, RTL designers working on a variety of semiconductor designs, ranging from data centers and CPUs to automotive ICs, can use PowerBaum to analyze and minimize power consumption in the early design stage for the highest impact. PowerBaum's fast power analysis capabilities can perform whole flow with batch process within a day – several orders of magnitude faster than current competitors.



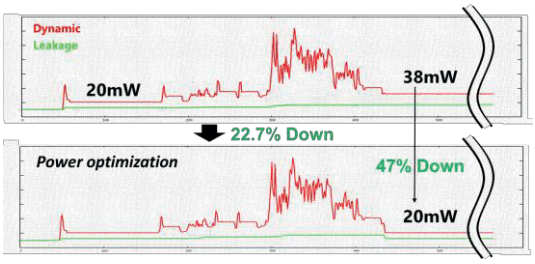
AI CHIP DESIGN

In the case of AI inference processors, designers are in a continuous struggle to improve the performance of the processor. Since battery technology has been stagnant, designers are forced to reduce the power of their inference processors. Besides, the ever-developing machine learning algorithms necessitate analyzing design's power weekly and often daily. PowerBaum provides the both speed and accuracy required by AI chip designers to optimize their design. A single power model generated by PowerBaum can be utilized to do power analysis with multiple PE (Processing Elements) instances giving designers the freedom to optimize the power consumption of AI chips.



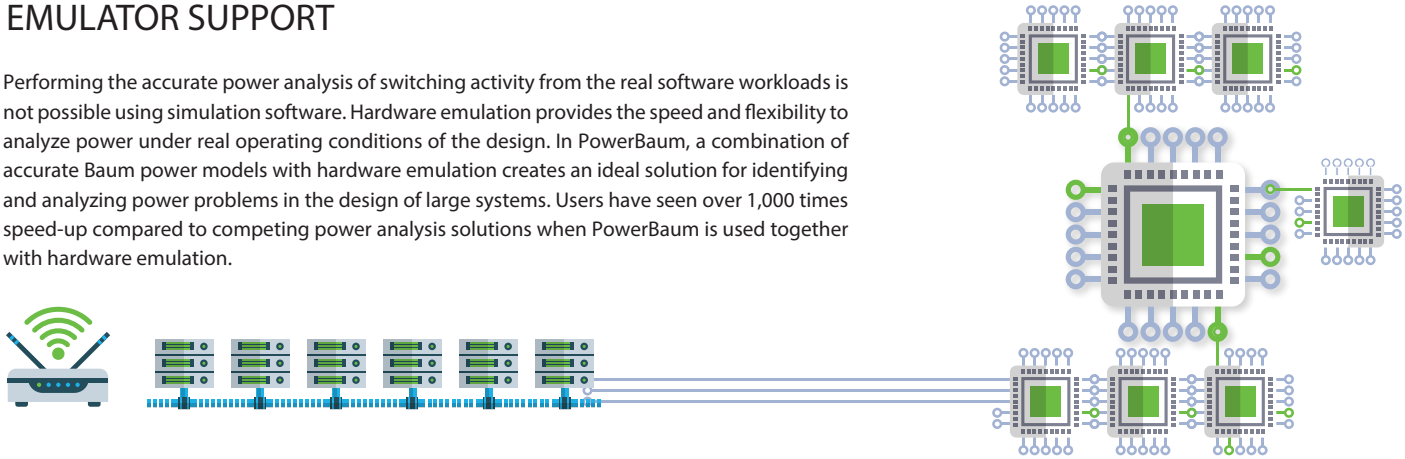
POWER DEBUGGING

In semiconductor design, the key to debugging the power issues is transient power analysis (analyzing the power waveform). Therefore, PowerBaum's ability to run transient power waveform analysis for different scenarios swiftly makes it a best-in-class power debugging platform for semiconductor design. The figure on the right illustrates critical power issues in a GPU design during the idle state. The designer was able to lower average power consumption by 22.7% with transient power analysis. By analyzing only average power or window of high activity, designer would not have found the problem.



EMULATOR SUPPORT

Performing the accurate power analysis of switching activity from the real software workloads is not possible using simulation software. Hardware emulation provides the speed and flexibility to analyze power under real operating conditions of the design. In PowerBaum, a combination of accurate Baum power models with hardware emulation creates an ideal solution for identifying and analyzing power problems in the design of large systems. Users have seen over 1,000 times speed-up compared to competing power analysis solutions when PowerBaum is used together with hardware emulation.



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